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Karen Cinq-Mars 11/18/03
(Signature & date)



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of _____:

November 18, 2003

Chidambarrao, Dureseti, et al.:

Group Art Unit: To Be Assigned

Serial No. 10/605,135:

Examiner: To Be Assigned

Filed: 9/10/03

International Business Machines Corporation
2070 Route 52
Hopewell Junction, NY 12533

TITLE: METHOD AND STRUCTURE FOR IMPROVED MOSFET'S USING POLY / SILICIDE GATE HEIGHT CONTROL

INFORMATION DISCLOSURE STATEMENT

Under 37 C.F.R. 1.56

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Under provisions of 37 C.F.R. 1.97 through 1.99 and pursuant to applicant's duty of disclosure under 37 C.F.R. 1.56, applicants respectfully bring the documents listed on the attached Form PTO-1449 to the attention of the examiner in charge of the above-identified application.

This citation does not constitute an admission that the cited references are relevant or material to the claims nor should it be construed as a representation that no other art than that identified exists. They are merely cited as constituting related art of which the applicant is aware.

It is respectfully requested that these documents be considered by the examiner and formally made of record in this application.

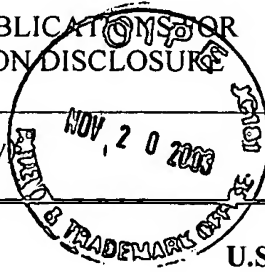
No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Dureseti Chidambarrao, et al.

By Joseph P. Abate 11-18-03
Joseph P. Abate
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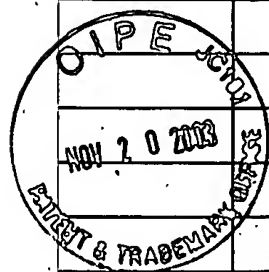
FIS920030184US1

FORM PTO-1449 (Modified)	ATTY. DOCKET NO. FIS9-2003-0184-US1	SERIAL NO. 10/605,135
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT: Chidambarrao, Dureseti, et al.	
(Use several sheets if necessary)	FILING DATE: 9/10/03	GROUP: Unassigned



REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	US 6,228,694 B1	5/8/2001	Doyle et al.			
	US 6,406,973 B1	6/18/2002	Lee			
	US 6,281,532 B1	8/28/2001	Doyle et al.			
	5,683,934	11/4/97	Candelaria			
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	US 3,602,841	8/31/1971	McGroddy			
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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

FIS920030184US1

Application Number

10/605,135

Applicant(s)

Chidambarao, Dureseti, et al.

Filing Date

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Group Art Unit

Unassigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

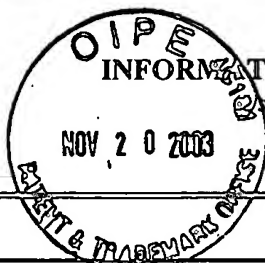
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		Novel Locally Strained Channel Technique for High Performance 55nm CMOS K. Ota, et al. 2002 IEEE, 2.2.1-2.2.4, IEDM 27.
		Local Mechanical-Stress Control (LMC): A New Technique for CMOS - Performance Enhancement A. Shimizu, et al. 2001 IEEE, 19.4.1-19.4.4, IEDM 01-433
		Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design Shinya Ito, et al. 2000 IEEE, 10.7.1-10.7.4, IEDM 00-247
		A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System -on-a- Chip Applications F. Ootsuka, et al. 2000 IEEE, 23.5.1-23.5.4, IEDM 00-575

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



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REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		NMOS Drive Current Reduction Caused by Transistor-Layout and Trench Isolation Induced Stress Gregory Scott, et al. 1999 IEEE, 34.4.1-34.4.4, IEDM 99-827
		Transconductance Enhancement in Deep Submicron Strained-Si n- MOSFETs Kern (Ken) Rim, et al. 1998 IEEE, 26.8.1-26.8.4, IEDM 98-707
		Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFET's K. Rim, et al. 2002 IEEE, 98-99, 2002 Symposium On VLSI Technology Digest of Technical Papers

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